120 Watt, 2GHz, Si LDMOS RF POWER TRANSISTOR FOR PCS BASE STATION APPLICATIONS

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Abstract

The structure and performance of a 120 Watt, 2GHz, Si RF LDMOS power transistor are described suitable for Personal Communication Systems base station power amplifiers operating in the 1.8-2.2 GHz frequency band. The high gain (10.6 dB at 120 Watts CW, 2GHz), and excellent linearity of this transistor, when operated in class-AB, (typically -30dBc two-tone intermodulation distortion at 120 Watts PEP) makes it eminently suitable for amplification of digitally modulated signals.

Introduction

Growth in Personnel Communications Systems in the 1.8 to 2.4GHz frequency band is rapidly accelerating worldwide. There are a number of different modulation and access schemes including Global System for Mobiles (GSM), Code Division Multiple Access (CDMA, IS-95), North American Digital Cellular or D-AMPS (IS-54 & IS136) and Wireless Local Loop (WLL). All these standards require linear RF amplifiers for the base stations and there is a need for cost effective high-power linear RF transistors for these applications. Silicon LDMOS transistors can provide higher gain and better linearity than silicon bipolar devices [1,2,3].

This paper describes the design and performance of a 120 Watt push-pull LDMOS transistor, operating in class-AB, with 10.6 dB of gain and 42% drain efficiency at 2 GHz. When driven with a two-tone signal, at 120 Watts PEP output power, the intermodulation distortion is -30dBc, gain is 11.7dB and drain efficiency 33%. Moreover, when this transistor is operated below half-power the intermodulation distortion is less than -40dBc. This is the highest power reported for any silicon RF LDMOS transistor operating in the PCS wireless communications bands.

Device Structure

RF LDMOS is a modified n-channel MOSFET specifically designed for both high frequency operation and power amplifier applications. Fig. 1 is a cross-section of the basic LDMOS structure. A p-type laterally diffused channel implant enhances the RF gain and prevents punchthrough at high drain-source voltages. The n+ source is strapped to a p+ sinker region by the source metal (Fig. 2); the p+ sinker is diffused to connect to the p+ substrate, which is itself bonded to the RF ground, thus minimizing common lead inductance and maximizing common source RF power gain. The source metal, isolated by a dielectric layer, also extends over the polysilicon gate to provide an inter-electrode shield, thereby minimizing drain-gate capacitance, C_{gd}. Epitaxial layer resistivity and thickness have been tailored in order that the length and doping in the lightly doped drain extension (NHV region) primarily determines the source-drain breakdown voltage, BV_{DSS}, which for this application typically exceeds 70 Volts. Rds(on) is also partially controlled by the doping level in the drain extension. A positive temperature co-efficient for Rds(on) contributes to the excellent reliability of this device structure under output mis-matched conditions.

The LDMOS dice are assembled in a push-pull package with a tee-section input match (Fig. 3). Wire-bonds form the series-L sections and MOS-capacitors the shunt-C element. Backside source connection on the die enables the die to be directly bonded to the CuW package thereby minimizing

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both the common-mode inductance and thermal resistance essential for high-power operation

Performance

Fig. 4 illustrates drive-up performance, under CW conditions, at 2GHz, in a class-AB narrow-band test circuit. Gain at 120 Watts is 10.6dB at a drain efficiency of 42%. Drive-up performance for an equal amplitude two-tone excitation is shown in Fig. 5. A quiescent drain bias of 850mA was set to give best overall linearity over a wide power range. At 120 Watts (PEP), 2GHz, power gain is 11.7dB and drain efficiency 33%.

Linearity performance is shown in Fig. 6. At 120 Watts PEP the 3rd order intermodulation distortion is -30dBc. Intermodulation distortion remains below -40dBc with the output power decreased >3dB. This illustrates the outstanding linearity of the RF LDMOS device structure. In RF amplifier applications, where the peak to average ratio is high, for example in multi-carrier amplifiers, this characteristic can be employed to great advantage in reducing error correction demands. Linearity in a class-AB LDMOS amplifier is a function of the quiescent bias current, which is illustrated in Fig. 7 where optimum linearity over 25dB range of output power is achieved with 850mA drain current. This corresponds to best gain flatness over the same dynamic range (Fig. 8).

The combination of push-pull operation and internal input matching increases the large-signal optimum source and load impedances compared to a single-ended transistor of the same power level and a similar complexity of internal matching. This results in good broadband performance as illustrated in Fig. 9. For a two-tone signal at 120 Watts PEP, gain flatness across the 1.93 to 1.99 GHz PCS band is <0.3dB peak to peak with a minimum gain of 11.1dB. Drain efficiency is 31% minimum and intermodulation distortion -30.5dBc maximum.

CDMA is an access scheme that has been adopted because of the anticipated high spectral efficiency. Each carrier is spread by a 1.2288MBps code sequence and up to 64 channels can be modulated on a single RF carrier. Modulation is QPSK. Fig. 10 shows the spectrum regrowth caused by non-linearities in the transistor operating at 25 watts average power for both 9 channels enabled (1 pilot, 1 paging, 1 sync and 6 traffic) and the full complement of 64 channels. Peak to average power ratio is 13.8dB with all channels enabled. Fig. 11 plots adjacent channel power ratio as a function of output power. IS-97A standard requires the total conducted spurious in any 30KHz band greater than 885KHz offset from the CDMA carrier center frequency not to exceed -45dBc. Under this restriction the transistor would be capable of handling a signal up to 25 Watts average power.

An alternative digital modulation scheme is defined by IS-54. Three voice channels are transmitted by TDMA over 6 time slots. The modulation is $\pi/4$ DQPSK. Fig. 12 illustrates the spectrum regrowth caused by non-linearities in the transistor operating at an average power level of 80 Watts. ACPR at this power level is -30dBc.

Summary

The results outlined in this paper demonstrate the suitability of RF LDMOS device technology for high power base station applications in the PCS frequency bands 1.8-2.0GHz. In a appropriate package, it has been demonstrated that multiple transistor cells can be combined to produce a transistor capable of amplifying a signal up to 120 Watts at 2GHz with 10.6dB power gain.

References

[1] Shaw, M. & Wood, A., "Characterization of a 2 GHz Submicron Bipolar 60 Watt Power Transistor with Single Tone, Multi-tone, and CDMA Signals," ARFTG meeting, June 1996.

[2] Camilleri, N et al; "Silicon MOSFETs, "The Microwave Device Technology for the 90's"; MTT-S International Microwave Symposium Digest 1993; pp. 545-548.

[3] Wood A, Dragon A. & Burger, W., "High Performance Silicon LDMOS Technology for 2GHz RF Power Amplifier Applications," IEDM Tech. Digest 1996, pp. 87-90.

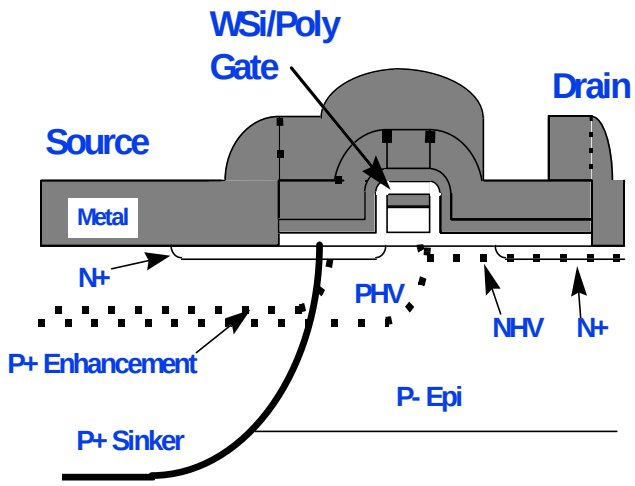

Figure 1. Cross-section of LDMOS Structure

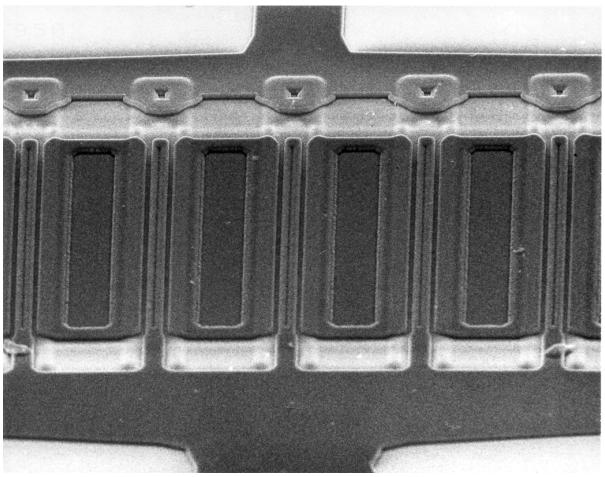

Figure 2. SEM of structure in a single cell.

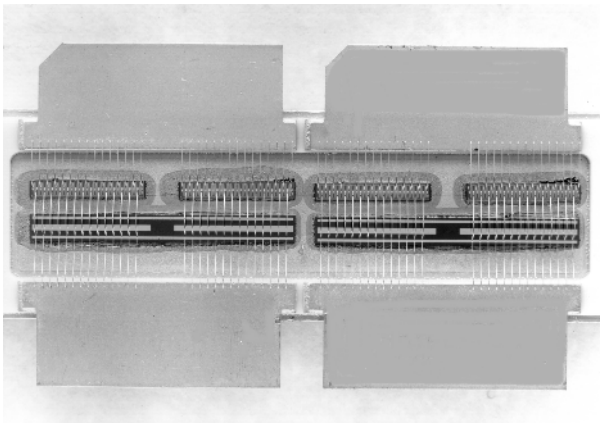

Figure 3. Photograph of 120 Watt transistor showing internal configuration

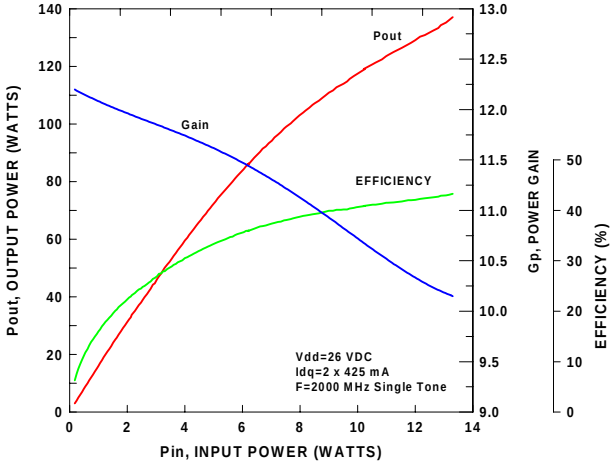

Figure 4. Single-Tone Output Power, Gain and Efficiency versus Input Power

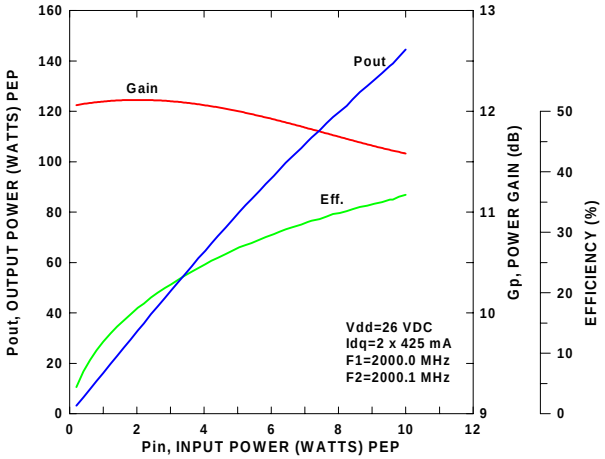

Figure 5. Two-Tone Output Power, Gain and Efficiency versus Input Power

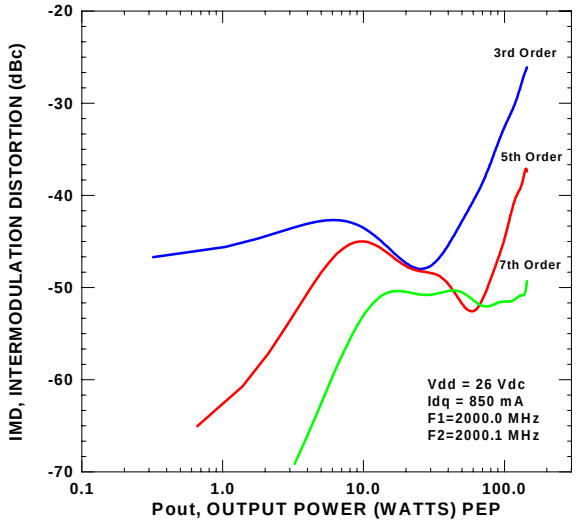

Figure 6. Two-Tone Intermodulation Distortion versus Output Power

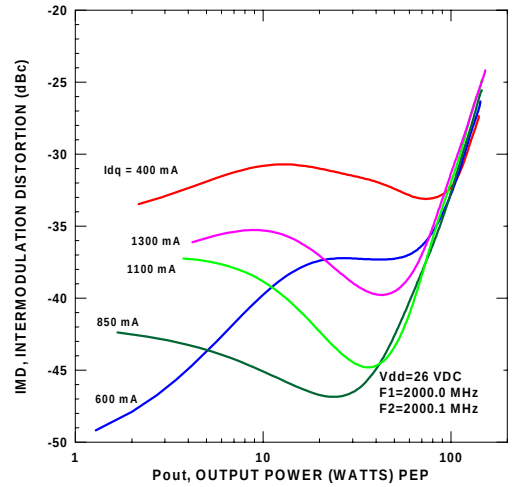

Figure 7. Class-AB Two-Tone Intermodulation Distortion versus Output Power as a function of drain bias.

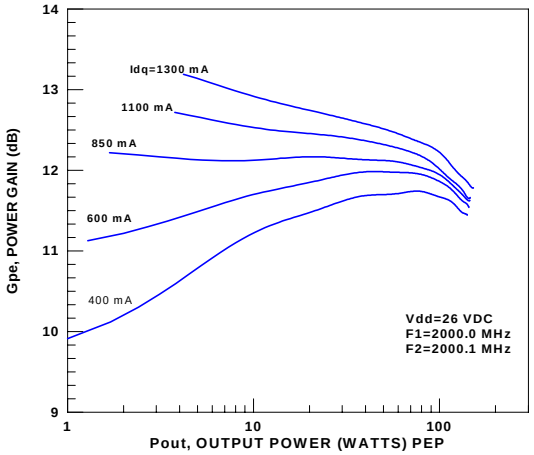

Figure 8. Class-AB Two-Tone Power Gain versus Output Power as a function of drain bias

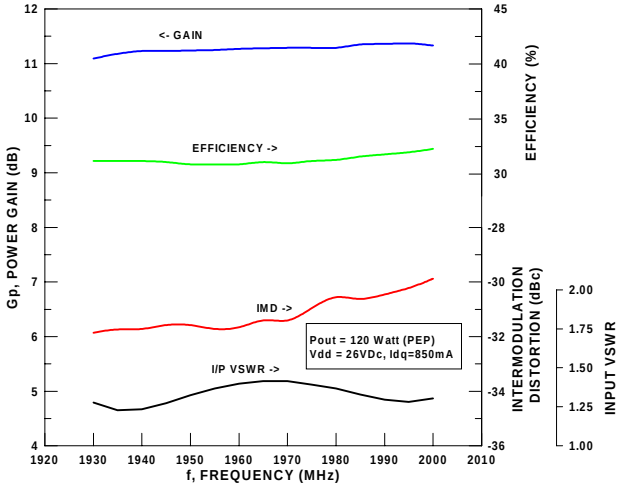

Figure 9. Class-AB Two-Tone 1.93-2.0GHz Broadband Performance.

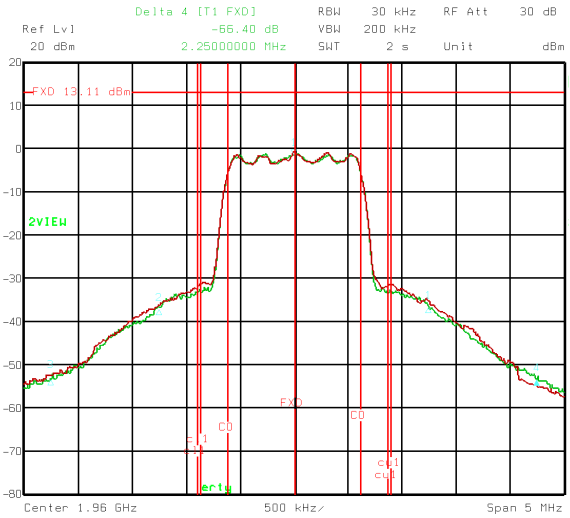

Figure 10. Spectrum Regrowth when driven by a 9ch & 64ch (IS-97A) CDMA signal.

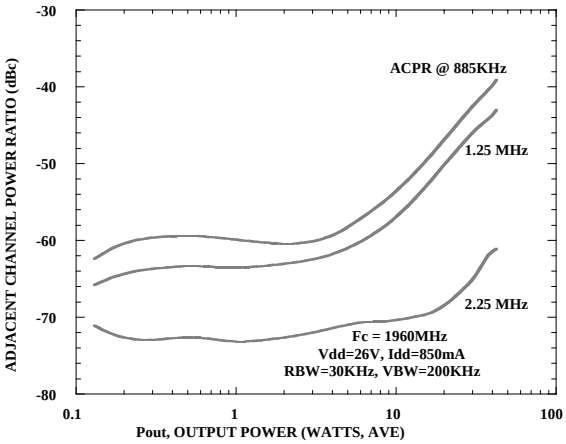

Figure 11. Adjacent Channel Power Ratio versus Output Power (IS-97A 64 Ch. CDMA signal).

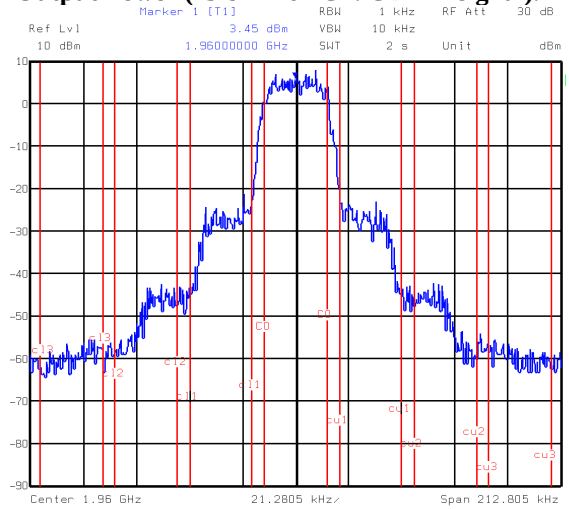

Figure 12. Spectrum Regrowth when driven by a NADC signal (1.96GHz, Pout=80W)